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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/615,705

07/13/2000

Yoko Horiguchi

Q60098

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01/21/2005

SUGHRUE, MION, ZINN, MACPEAK & SEAS
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EXAMINER

NADAV, ORI

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/615,705

Applicant(s)

HORIGUCHI, YOKO

Examiner

ori nadav

Art Unit

2811

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 November 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8, 10-13, 15, 17, 19, 21-23 and 25-32 is/are pending in the application.
- 4a) Of the above claim(s) 2, 4-7, 11, 13, 15, 17 and 19 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 3, 8, 10, 12, 21-23 and 25-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 3, 8, 10, 12, 21-23 and 25-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuya (Jp 11-154733) in view of Merritt (5,828,095).

Furuya teaches in figure 6 a semiconductor device comprising a capacitor 613 connected between a power source wire 600 and a ground potential wire 603, a power source terminal 605 to which voltage is applied, a ground terminal 606 to which the ground potential wire is connected, and an ESD being a MOSFET connected in parallel with the capacitor, and a wire resistance of the ground potential between the ESD element connection point and the ground terminal 606 being larger than that between the ESD element connection point and the MOS capacitor's connection point.

The wire resistance of the ground potential between the ESD element connection point and the ground terminal 606 is larger than that between the ESD element connection point and the capacitor's connection point, because a wire resistance is directly proportional to the length of the wire, and the distance between the ESD element

connection point and the ground terminal 606 is larger than that between the ESD element connection point and the capacitor's connection point.

Furuya does not teach in the embodiment of figure 6 that capacitor 613 is a MOS capacitor and does not teach supplying the power voltage through a power source conversion circuit.

Furuya teaches that capacitors of the described invention are MOS capacitors (abstract).

Merritt teaches supplying a power voltage through a power source conversion circuit (column 1, lines 21-23).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a MOS capacitor in the embodiment of figure 6 in Furuya's device and to supply the voltage in Furuya's device through a power source conversion circuit, in order to form the device as taught by Furuya, and in order to provide the proper voltage to the device, respectively.

Regarding the claimed limitations of electrostatic protection element protecting said semiconductor integrated circuit device from electrostatic breakdown due to discharge of electrostatic charge accumulated on said semiconductor integrated circuit device according to a charged device model, these features are inherent in prior art's device, because these features are the known function of an ESD protection element.

Art Unit: 2811

Regarding claims 3 and 22, Furuya teaches no other diffusion layer except the ESD element is connected on the ground potential wire between the ground terminal and the connection point on the ground potential wire with one end of the MOS capacitor.

Regarding claims 10 and 25, although Furuya does not explicitly disclose the ESD element clamps a voltage applied to both terminals at a clamp voltage which is lower than the dielectric breakdown voltage of the MOS capacitor, this feature is inherent in Furuya's device, because Furuya's structure is identical to the claimed structure.

Regarding claims 12 and 26, Furuya teaches in figure 5 an ESD MOSFET, the drain of which is connected to the power source wire and the source and gate of which are connected to the ground potential wire.

Regarding claims 27, 29-30 and 32, Furuya teaches an ESD element comprising a bipolar transistor or a diode.

Regarding claims 28 and 31, Furuya teaches an ESD element comprising a bipolar transistor or a diode. it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an ESD element comprising a thyristor in Furuya's device, because thyristor is a well-known ESD protection device.

Response to Arguments

3. Applicant argues that Furuya does not teach protecting the device from ESD breakdown due to a charged device model, because Furuya teaches protection from human body model or a machine model.

Prior art's device protects the internal circuits from an ESD breakdown, regardless of the source of the electric charges. This includes protection from external electrical charges originated from the package or the lead frames of the device. Therefore, prior art's device provides protection also from ESD breakdown due to a charged device model. Furthermore, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). In this case, prior art's device is able to protect the internal circuits from external electrical charges originated from the package or the lead frames of the device, as claimed.

4.

5. Applicant argues that figure 6 of Furuya does not suggest that the MOS device 609 is positioned relative to capacitor 613 such that the wire resistance of the ground potential between the ESD element connection point and the ground terminal is

Art Unit: 2811

larger than that between the ESD element connection point and the capacitor's connection point, because the courts found that a drawing having dimensions on the order of a few thousands of an inch can not be scaled off to show that any particular distance is exactly equal.

The examiner does not use figure 6 of Furuya to deduce a specific dimension or to scale off to show that a particular distance is exactly equal to another distance. The examiner uses figure 6 of Furuya to show the relative distances between various connection points, and does not rely on exact measurements of distances. Note that although the drawings of a patent are not to scale, the drawings together with the description of the article, can be relied on, for what they would reasonably teach one of ordinary skill in the art. In re Wright, 193 USPQ 332 (CCPA 1977).

The broad recitation of the claim does not preclude the wire resistance of the ground potential between the ESD element connection point and the ground terminal to be larger than the wire resistance between the ESD element connection point and the capacitor's connection point ($R_1 > R_2$), due to their relative lengths. Note that prior art references of record only teach that $R_1 > R_2$ due to the relative lengths of the wiring, but does not teach that $R_1 > R_2$ due to any other factor.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**



O.N.
January 20, 2005

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800